

Appln No. 09/923,676

Amdt date April 13, 2005

Reply to Office action of January 13, 2005

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1-15. (Cancelled)

16. (Currently Amended) A receiver for intercepting a modulated radio signal in a first mode or and second mode, the receiver comprising:

[a plurality of] first and second antennas having different directionality to produce [a] corresponding [plurality of] first and second input signals;

means for evaluating the quality of the [plurality of] first and second input signals;

[a plurality of] first and second signal processors connected to the [respective] one or both of the first and second antennas for demodulating the respective [plurality of] first and second input signals;

a tuner in each of the first and second signal [processor] processors, the tuners being set to different frequencies in the first mode and the same frequency in the second mode;

a utilization circuit;

[means for setting the tuners to different frequencies in a first mode of operation;

means for setting the tuners to the same frequency in a second mode of operation;]

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means in the first mode for connecting both of the signal processors to the utilization circuit irrespective of the quality of the input signals; and

means responsive to the evaluating means in the second mode for connecting one of the signal processors to the utilization circuit based on the quality of the input signals.

17. (Previously Presented) The receiver of claim 16, in which the connecting means responsive to the evaluating means in the second mode comprises a switch.

18. (Original) The receiver of claim 17, in which the utilization circuit has forward error correction means.

19. (Original) The receiver of claim 18, in which the radio signal comprises a digital television signal with QAM modulation and the utilization circuit comprises a VSB processor with forward error correction.

20. (Previously Presented) The receiver of claim 19, in which the utilization circuit additionally has an MPEG decoder.

21-30. (Canceled)

31. (Previously Presented) The receiver of claim 16, in which the utilization circuit comprises a PIP chip to which both of the signal processors are coupled in the first mode and means for connecting the PIP chip to the TV display.

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32. (Previously Presented) The receiver of claim 31, in which the utilization circuit additionally comprises combining means to which both signal processors are coupled in the second mode and means for connecting the combining means to the TV display.

33. (Previously Presented) The receiver of claim 31, in which the utilization circuit additionally comprises selecting means to which both signal processors are coupled in the second mode and means for connecting one of the signal processors to the TV display